Hall Ticket Number:

Code No. : 13651 S N/O

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (I.T.) III-Semester Supplementary Examinations, August-2023

Digital Electronics and Logic Design

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Draw the logic circuit symbol of a three input AND gate and give its truth table.	2	1	1	1
2.	If 52/4 = 12 find the base of the number system.	2	1	1	1
3.	Draw the logic circuit diagram of a 2x1 Multiplexer.	2	1	2	1
4.	Draw the logic circuit diagram of a half adder circuit.	2	1	2	1
5.	Give the excitation table of a SR flip flop.	2	1	3	1
6.	What is logic race condition and how it can be avoided	2	1	3	1
7.	What is state reduction? What is achieved by doing state reduction?	2	1	4	1
8.	What is state equivalence principle?	2	1	4	1
9.	Define clock skew.	2	2	5	1
10.	What are ASM charts?	2	2	5	1
	Part-B (5 × 8 = 40 Marks)				
11. a)	Draw K map ans simplify the following $F(A,B,C,D)= \Sigma(0,2,4,6,8, 10,12,14,15)$	4	3	1	1
b)	Simplify the following Boolean function and implement them with NAND gates AB' + ABD + ABD' + A'C'D' + A'BC'	4	3	1	1
12. a)	Implement a full subtractor circuit with two half subtractors and an OR gate.	4	3	2	1
b)	Implement a Full adder circuit using VHDL.	4	4	5	1,3
13. a)	With a neat circuit digarm explain the operation of a Master Slave J K flip flop.	4	3	3	1
b)	What is Characteristic equation of a flip flop? Derive the characteristic equation of J K flipflop	4	3	3	1,2

Contd... 2

14. a)	Illustrate the procedure of state reduction by taking a suitable example.	4	4	4	2
b)	Distinguish between Mealy and Moore sequential circuits.	4	2	4	1
15. a)	List and explain the different types of hazards in logic circuits.	4	2	3	1
b)	Explain about the different elements of an ASM chart.	4	2	4	1
16. a)	Simplify the following in POS form: $F(w,x,y,z)= \Sigma(2,3,4,5,6,7,11,14,15)$	4	2	1	1
b)	Implement the following function s using a PLA $F1(A,B,C)= \Sigma m(0,1,2,4)$ $F2(A,B,C)= \Sigma m(0,5,6,7)$	4	3	2	3
17.	Answer any ***two*** of the following:				
a)	Design a synchronous modulo -6 counter using T flipflops	4	4	3	3
b)	Design a two bit ripple down counter using negative edge triggered J K flip flops.	4	4	4	3
c)	Implement a D flip flop in VHDL	4	4	5	3

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	25%
iii)	Blooms Taxonomy Level – 3 & 4	55%

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